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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/774,888

02/01/2001

Jun Koyama

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EXAMINER

WEISS, HOWARD

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 09/774,888	Applicant(s) KOYAMA ET AL.	
	Examiner Howard Weiss	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 October 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1, 77-84, 87-90, 93-103, 105, 106 and 108-153 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 77-84, 87-90, 93-103, 105, 106 and 108-153 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Attorney's Docket Number: 740756-2255

Filing Date: 2/1/01

Continuing Data: RCEs established 3/27/2003, 8/19/2004, 10/13/2005, 11/22/2006 and
10/5/2007

Claimed Foreign Priority Date: 2/1/00 (JPX)

Applicant(s): Koyama et al. (Kato)

Examiner: Howard Weiss

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/5/2007 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Initially, and with respect to Claims 1, 77 to 80 and 122 to 125, note that a "product by process" claim is directed to the product per se, no matter how actually made. See *In re Thorpe et al.*, 227 USPQ 964 (CAFC, 1985) and the related case law cited therein which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. As stated in Thorpe,

even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. *In re Brown*, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972); *In re Pilkington*, 411 F.2d 1345, 1348, 162 USPQ 145, 147 (CCPA 1969); *Buono v. Yankee Maid Dress Corp.*, 77 F.2d 274, 279, 26 USPQ 57, 61 (2d. Cir. 1935).

Note that Applicant has burden of proof in such cases as the above case law makes clear.

4. Claims 1, 77, 79 to 81, 83, 84, 87,89, 90, 93, 95 to 98, 100 to 103, 106, 108 to 111, 113 to 116 and 122 to 149 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (JP 11-154714 and the Derwent Translation of this document) and Tsutsumi (U.S. Patent No. 5,844,274).

Yamazaki et al. show most aspects of the instant invention (e.g. Figures 1 to 8) including:

- a memory cell array with memory cells formed in a n x m matrix with X-address **101** and Y-address **102** decoders electrically connected to signal lines **Cnn,Dnn, Amm,Bmm**
- each cell containing a memory thin film transistor (MTFT) **Tr1** and a switching thin film transistor (STFT) **Tr2**
- said MTFT including:

- a first semiconductor active layer **202** formed on an insulating substrate **201**, having a first thickness **d1** and comprising a channel forming region **205**
- a first insulating film **211**, a conductive layer (i.e. floating gate electrode) **213** adjacent to the first semiconductive active layer and used to trap electrons, a second insulating film **214** of an oxide and a control gate electrode **215**
- a wiring **825** for connecting the control gate to a first single line **809**
- said STFT including:
 - a second semiconductor active layer **206** formed on an insulating substrate **201** and having a second thickness **d2**
 - a gate insulating layer **212** and a gate electrode **217**
 - a second signal line **810** connected to said gate electrode
- where in **d1** is thinner (i.e. smaller) than **d2** (Paragraphs 0058 and 0059)

Yamazaki et al. does not show the floating gate comprising silicon with one conductivity, the control gate comprising a laminate of three films: TaN/W/WN and each film comprising the inert element xenon.

Tsutsumi teaches (e.g. Column 17 Lines 14 to 20) it is common, and therefore obvious, to form gate electrodes of layers comprising TaN/W/WN. It would have been obvious to a person of ordinary skill in the art at the time of invention to form gate electrodes of layers comprising TaN/W/WN as taught by Tsutsumi in the device of Yamazaki et al. since it is common in the art to do so. Also, it is common to use silicon with one conductivity (e.g. doped polysilicon) as floating gate material.

As to the grounds of rejection under "Product-by-Process", how the first and second films are formed, either by sputtering using an inert gas or by some other means, pertains to intermediate process steps which does not affect the final device

structure. See MPEP § 2113 which discusses the handling of "product by process" limitations.

5. Claims 117, 118, 120, 121 and 150 to 153 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. and Tsutsumi, as applied to Claim 1 above, and further in view Akbar (U.S. Patent No. 5,656,845).

Yamazaki et al. and Tsutsumi show most aspects of the instant invention (Paragraph 4) except for the first and second semiconductor layer in a common semiconductor island. Akbar teaches (e.g. Figures 1 and 8 to 10) to form first and second semiconductor layers in a common semiconductor island (i.e. layer) **122** to provide memory cells with improved performance and reliability (Column 2 Lines 19 to 22). It would have been obvious to a person of ordinary skill in the art at the time of invention to form first and second semiconductor layers in a common semiconductor island as taught by Akbar in the device of Yamazaki et al. and Tsutsumi to provide memory cells with improved performance and reliability.

6. Claims 78, 82, 88, 94, 99, 105 and 112 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. and Tsutsumi, as applied to Claim 1 above, and further in view of Koyama (U.S. Patent No. 5,793,344).

Yamazaki et al. and Tsutsumi show most aspects of the instant invention (Paragraph 4) except for the semiconductor device comprising a pixel portion over the substrate, a source wiring driver circuit for driving the pixel portion over the substrate and a gate wiring driver circuit for driving the pixel portion over the substrate for controlling the non-volatile memory circuit all part of an LCD of a video camera. Koyama teach (Paragraph 3) to use the memory device with the listed devices to produce a high quality display device (Column 7 Lines 55 to 61). It would have been obvious to a person of ordinary skill in the art at the time of invention to use the memory device of

Yamazaki et al. and Tsutsumi with the listed devices of Koyama to produce a high quality display device.

7. Claim 119 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al., Tsutsumi and Koyama, as applied to Claim 78 above, and further in view of Akbar.

Yamazaki et al., Tsutsumi and Koyama show most aspects of the instant invention (Paragraph 6) except for the first and second semiconductor layer in a common semiconductor island. Akbar teaches (e.g. Figures 1 and 8 to 10) to form first and second semiconductor layers in a common semiconductor island (i.e. layer) **122** to provide memory cells with improved performance and reliability (Column 2 Lines 19 to 22). It would have been obvious to a person of ordinary skill in the art at the time of invention to form first and second semiconductor layers in a common semiconductor island as taught by Akbar in the device of Yamazaki et al., Tsutsumi and Koyama to provide memory cells with improved performance and reliability.

Response to Arguments

8. Applicant's arguments with respect to Claims 1, 77 to 84, 87 to 90, 93 to 103, 105, 106 and 108 to 153 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(571) 273-8300**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Howard Weiss at **(571) 272-1720** and between the hours of 7:00 AM to 3:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via Howard.Weiss@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on **(571) 272-1705**.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at **866-217-9197** (toll-free).

12. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/326, 347; 365/ 185.05	thru 12/18/2007
Other Documentation: none	
Electronic Database(s): EAST	thru 12/18/2007

HW/hw
20 December 2007

/Howard Weiss/
Primary Examiner
Art Unit 2814